Claims:

A listing of the claims has been included for reference. Claims 24, 30, 32, 37, 38, 41, and 47 have been amended. Claims 1-23 were previously canceled. Claims 33, 34, 43, 44, 48, and 49 are currently being cancelled.

Listing of Claims:

Claims 1-23. (Cancelled)

24. (Currently Amended) An apparatus comprising:

a controller, before controller initialization in response to a power-up or a soft reset of the apparatus, configured to generate

an unencoded chip select word in response to **an address for a boot device, wherein the unencoded chip select word comprises the lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the boot device** ~~**a default unencoded chip select mode**~~,

an encoded chip select word in response to **an address for a boot device, wherein the encoded chip select word comprises the lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the boot device** ~~**a default encoded chip select mode**~~; and

wherein the encoded chip select word and the unencoded chip select word select a same boot device.

25. (Previously Presented) The apparatus of claim 24, wherein the controller comprises a memory controller to generate the encoded chip select word and the unencoded chip select word.

26. (Previously Presented) The apparatus of claim 25, wherein the memory controller comprises an address decoder to generate the encoded chip select word and the unencoded chip select word.

27. (Previously Presented) The apparatus of claim 24, wherein the controller initialization comprises configuration of the controller to operate in an encoded chip select mode or in an unencoded chip select mode.

28. (Previously Presented) The apparatus of claim 27, wherein the controller comprises a configuration store to store configuration data to configure the controller to operate in an encoded chip select mode or in an unencoded chip select mode.

29. (Previously Presented) The apparatus of claim 24, wherein the boot device comprises a memory device.

30. (Currently Amended) The apparatus of claim 24, wherein the unencoded chip select **word** ~~**world**~~ comprises a first bit pattern and the encoded chip select **word** ~~**world**~~ comprises a second bit pattern and the first bit pattern includes the second bit pattern.

31. (Previously Presented) The apparatus of claim 30, wherein the lowest order of bits of the first bit pattern include the second bit pattern.

32. (Currently Amended) The apparatus of claim 24, wherein ~~the controller to generate the encoded chip select world and the unencoded chip select world in response to an address for a boot code nub and~~ the boot device stores ~~comprises~~ a ~~the~~ boot code nub.

33. (Cancelled)

34. (Cancelled)

35. (Previously Presented) The apparatus of claim 24 wherein the encoded chip select word is generated according to an encoding scheme to assign numbers to a plurality of boot devices, the numbers to range from one to a number greater than one.

36. (Previously Presented) The apparatus of claim 35 wherein the encoded chip select word is to encode the number one.

37. (Currently Amended) The apparatus of claim 24, wherein the controller, in response to an address for a boot code nub that does not map to the ~~single~~ boot device, converts the address to an address that does map to the ~~single~~ boot device.

38. (Currently Amended) A system comprising:

a plurality of devices comprising a **boot** device storing a boot code nub, and

an apparatus, comprising a controller, in response to an address for the boot code nub and during a power-up or soft reset of the apparatus, configured to generate,

an unencoded chip select word in response to **the address, wherein the unencoded chip select word comprises a lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the boot device storing the boot code nub** ~~a default unencoded chip select mode~~,

an encoded chip select word in response to **the address, wherein the encoded chip select word comprises a lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the boot device storing the boot code nub** ~~a default encoded chip select mode~~; and

wherein the encoded chip select word and the unencoded chip select word select a same boot device.

39. (Previously Presented) The system of claim 38 wherein

the device storing the boot code nub is coupled to the apparatus via a predetermined chip select line,

each of the other devices of the plurality of devices is coupled to the apparatus via a separate chip select line; and

wherein the apparatus activates the predetermined chip select line coupled to the device storing the boot code nub, regardless of whether the chip select word is encoded or unencoded.

40. (Previously Presented) The system of claim 38 further comprising a chip select decoder coupled to the apparatus and coupled to each of the devices of the plurality of devices via a separate chip select line, wherein,

the chip decoder activates the chip select line of the device with the boot code nub in response to receiving the chip select word, regardless of whether the chip select word is encoded or unencoded.

41. (Currently Amended) A method comprising:

generating on a controller, in response to an address for the boot code nub and during a power-up or a soft reset of the apparatus,

an unencoded chip select word in response to **the address, wherein the unencoded chip select word comprises a lowest order active chip select bit that corresponds to a predetermined chip-select line used to select a boot device storing the boot code nub** ~~a default unencoded chip select mode~~,

an encoded chip select word in response to **the address, wherein the encoded chip select word comprises a lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the boot device storing the boot code nub** ~~a default encoded chip select mode~~; and

wherein the encoded chip select word and the unencoded chip select word select a same boot device.

42. (Previously Presented) The method of claim 41, further comprising executing the boot code nub, and

in response to executing the boot code nub, updating one of the default unencoded chip select mode and the default encoded chip select mode to one of an unencoded chip select mode and an encoded chip select mode.

43. (Cancelled)

44. (Cancelled)

45. (Previously Presented) The method of claim 41, wherein generating the chip select word comprises generating the chip select word as an encoded chip select word according to an encoding scheme that assigns numbers to a plurality of boot devices, the numbers ranging in magnitude from one to a number greater than one.

46. (Previously Presented) The method of claim 45, wherein the encoded chip select word encodes the number one.

47. (Currently Amended) A machine readable physical storage medium comprising a plurality of instructions that, in response to being executed result, in a controller

generating, in response to an address for the boot code nub and during a power-up or a soft reset of the apparatus,

an unencoded chip select word in response to **the address, wherein the unencoded chip select word comprises a lowest order active chip select bit that corresponds to a predetermined chip-select line used to select a boot device storing the boot code nub** ~~**a default unencoded chip select mode**~~,

an encoded chip select word in response to **the address, wherein the encoded chip select word comprises a lowest order active chip select bit that corresponds to a predetermined chip-select line used to select a boot device storing the boot code nub** ~~**a default encoded chip select mode**~~; and

wherein the encoded chip select word and the unencoded chip select word select a same boot device.

48. (Cancelled)

49. (Cancelled)